



**Detailed Specification of the  
FAIR Accelerator Control System Component  
„Interlock System“**

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**Abstract**

This document describes the Detailed Specification of the accelerator control system component "Interlock System". This work package is part of the "Machine Protection and Safety Systems" work package and covers the PSP code 2.14.10.11.2.

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## 1. Purpose and Classification of the Document

The purpose of this document is to specify the Accelerator Control System component "Interlock System" for FAIR (PSP code 2.14.10.11.3).

The Interlock System work package is as a sub element of the "Machine Protection and Safety Systems" work package (PSP code 2.14.10.11).

This document is the most detailed type of document in the hierarchy of Control System specifications.

Whenever regulations and requirements are specified in the General Specifications, Technical Guidelines or Common Specifications of the Control System they are only referenced in this document. The related documents are listed in Appendix II.

No legal or contractual conditions are treated in this document. All related information is given in the General Specifications for FAIR.

### 1.1. Responsibilities

The responsibilities with respect to changes and modifications of the present document are entirely in the hands of the Controls Department of the GSI Helmholtz Centre for Heavy Ion Research GmbH (GSI) Darmstadt.

For initial information please contact the administration of the Controls Department.

Further information on the organigram, names of responsible persons and task leaders, as well as the agreed document release and approval procedure is summarized in the organizational note 'Controls Project for FAIR'.

### 1.2. Classifications of Requirements

The following definitions of requirement classifications are being used throughout the document:

- **"Must"** or **"shall"** or **"is required to"** are used to indicate mandatory requirements, strictly to be followed in order to conform to the standard and from which no deviation is permitted.
- **"Must not"** or **"shall not"** mean that the definition is an absolute prohibition of the specification.
- **"Should"** or **"is recommended"** is used to indicate that among several possibilities one is recommended as particularly suitable, without mentioning or excluding others or that a certain course of action is preferred but not required.
- **"Should not"** or **"is not recommended"** mean that there may exist valid reasons in particular circumstances when the particular behavior is acceptable or even useful, but the full implications should be understood and the case carefully weighted before implementing any behavior described with this label.
- **"May"**, which is equivalent to **"is permitted"**, are used to indicate a course of action permissible within the limits of the standard.

## **2. Scope of the Technical System**

### **2.1. System Overview**

The Interlock System is part of the “Machine Protection” work package, which protects the accelerator from damage by misled beams and e.g. minimizes radioactive contamination by unforeseen beam deposition.

As integral part of the Control System the Interlock System reflects an orthogonal aspect and imposes requirements on several components of the control system. It closely interacts with e.g. the equipment layer, the front-end controllers, the timing master and its process descriptions, the Settings Management System [10] and the application layer. Therefore, also the detailed specifications for the above mentioned components (Timing System, Front-end Systems and Machine Protection) are to be considered.

The Interlock System concentrates various interlock source signals, processes them and triggers the appropriate reactions. Possible reactions can be to either switch the beam to a pilot beam or disable further beam production of this or all beam production chains, plus eventually dump the beam in an upstream accelerator.

The Interlock System described here is intended for usage in all sections of FAIR. Requirements for the interlock system can be categorized as follows:

- The interlock system must transport interlock information from various interlock sources to a central interlock processor in a fast and reliable way.
- The central interlock processor interacts closely with the central scheduler. The timing master as central scheduler must react on interlocks according to dynamically programmed decision trees provided by the Settings Management System. Therefore the interlock processor must be set up specifically for the beam production chains that are currently set up in the facility, and must inform the timing master about summary interlock conditions.
- The operators need to have a static status overview of the accelerator complex including the information about the present interlocks and a dynamic overview about changes to the scheduling caused by the interlock system.

Based on these perspectives, the following three components of the interlock system can be identified: the operation layer, the processing layer, and the signal pickup layer. This document defines the specification of the corresponding components of the Interlock System in dedicated subsections, see chapter 3.

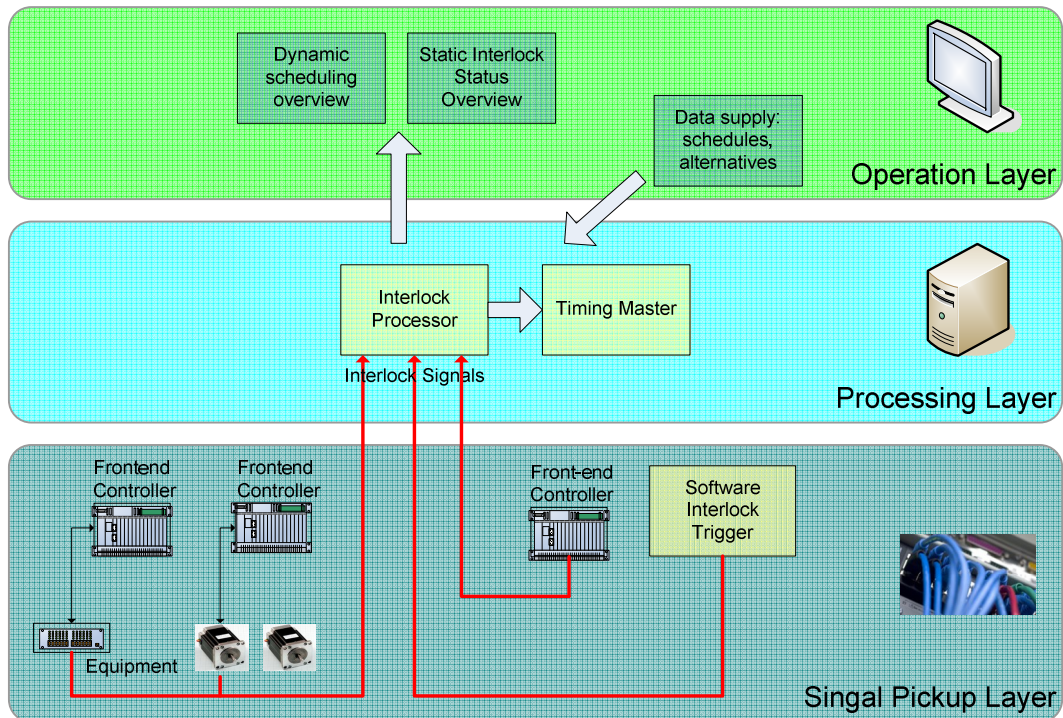


Figure 1: Interlock System Overview

## 2.2. Limits of the System and Environment

### 2.2.1. Limits

The interlock system is part of the machine protection system, which protects the accelerator from damage by misled beams.

It is not the responsibility of the interlock system to guarantee internal safety of any equipment, instead, equipment must protect itself (e.g. against settings out of defined limits or against damages by environmental conditions like overheating).

### 2.2.2. Interfaces

The interlock system has interfaces to many other components of the control system like the timing system, equipment, software on front-end controllers, and central software services, see also chapter 3.1.

### 2.2.3. Environment

Hardware components, like inputs to connect to the interlock output of the equipment, and the interlock processing unit, may be installed either close to the equipment or in electronics rooms in the facility. Electronic components have to run in the general environmental conditions of the FAIR maintenance buildings. General air conditioning must not be expected.

## 2.3. Basis of Concept

### 2.3.1. Functional Requirements

Definition of the term Interlock System: “The interlock system concentrates various interlock source signals, processes them and triggers the appropriate reactions.”

An interlock itself is a state that represents the inability of a component to handle the beam properly or represents the indication of a malfunction, e.g. the detection of bad beam conditions.

The Interlock System fulfills the following functional requirements:

Number	Description of the Requirement
IL_010	The interlock system must guarantee that a fault condition which is signaled e.g. by equipment or software processes is transported and processed within a given time.
IL_020	Interlock information must be communicated to the timing master whenever they occur, especially they must be provided anytime, also <i>during</i> an execution of a beam production chain.
IL_030	The interlock system must be configurable for different usages of the accelerator (e.g. commissioning, high intensity beam, shutdown).
IL_040	The interlock system must distinguish between beam-dependent and non beam-dependent interlock conditions. Beam-dependent interlocks affect only specific beam production chains, non beam-dependent interlocks affect all beams.
IL_050	Present interlocks (masked and/or unmasked) must be displayed to the operators. It must be possible to filter displayed interlocks (by timestamp (newest / oldest first), physical machine, beam pattern, beam production chain and interlock source).
IL_060	Interlocks must not “disappear” automatically, instead, they need to be acknowledged / cleared by an operator. <sup>1</sup>
IL_070	It must be possible for the operator to temporarily mask interlock sources in his own responsibility.
IL_080	The interlock system must provide the present interlock status to other interested clients (e.g. the Dynamic Scheduling Overview Application).
IL_090	Interlocks must be archived in a long term storage.

Table 1: List of Functional Requirements

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<sup>1</sup> It must be taken into account that already most of the equipment will latch their interlock status themselves. Such an interlock must be cleared directly at the equipment.

### 2.3.2. Non-functional Requirements

The Interlock System fulfills the following non-functional requirements:

Number	Description of the Requirement
IL_100	The interlock system must be scalable and grow together with the facility while providing the full functionality from the beginning.
IL_110	Interlock transportation and processing must not take more than about 100 ms (half the time of the fastest SIS18/SIS100 cycles).
IL_120	If collection of interlock inputs in some areas is out of operation, these inputs must be considered as if they are in interlock state. Interlock processing must be fully operational.
IL_130	The interlock system must allow maintenance of parts of the system, while the rest of the system must remain fully operational.

Table 2: List of Non-functional Requirements

### 2.3.3. General Constraints

All access limitations, e.g. restricting masking of interlocks to authorized personnel, must be based on standard functionality provided by the main contractor.

All GUIs must comply with the GUI Guidelines [8].

### 2.3.4. Architectural Principles

The Software Architecture Guideline for the Control System [7] fully applies.

## 3. Technical Specifications

### 3.1. Signal Pickup Layer

Sources and targets of the interlock system are hardware and software components. It must be possible to connect all sources and targets to the interlock system. Especially for connecting hardware components, the FAIR Technical Guideline F-TG-C-03e [2] and the guidelines [3], [4], [5] apply.

Typical sources, that need to be connected, are:

- Equipment (e.g. for notification of temperature problems)
- Equipment which may be inserted into the beam path (e.g. insertion of a beam instrumentation element into a high intensity beam has to be handled as an interlock condition)
- Software processes like monitoring processes, that check the beam quality
- Front-end software, which e.g. monitors equipment functionality
- Specific sources like
  - The autonomous beam dump system of SIS100

The interlock system must provide inputs to connect hardware interlock signals according to the FAIR Technical Guideline F-TG-C-03e [2] to the interlock system.

The interlock system must add a timestamp with millisecond accuracy to an interlock in the first signal processing unit within the interlock system that detects the interlock. The interlock system therefore must use a time server that is provided by the General Machine Timing System [6].

The interlock system must provide static configuration to assign hardware interlock inputs to devices in the accelerator facility, identified by the devices' nomenclatures. It must be possible to assign several hardware inputs to the same device nomenclature.

All static configurations must be stored in non-volatile way in the interlock system. Set-up and modification of the assignment must be protected against unwanted manipulations, using standard functionality provided by the main contractor.

Interlocks which are generated by software components provide great flexibility and will be used in many cases. The interlock system must provide means that software processes can signal interlock states reliably to the interlock system.

The interlock system must support and provide appropriate means to identify the software interlock source and to assign such software generated interlock signals to activities and layout of the facility: At least assignment of software generated interlocks to beam production chains and sections of the facility, as described in chapter 3.2, must be supported.

One software component may generate several interlock signals. The interlock system must support to assign each signal to a different beam production chain and facility section.

The interlock system must support to assign the same software generated interlock signals to several beam production chains and facility sections.

The interlock system needs to connect all interlock sources. The interlock system must foresee that additional sources may be added at a later stage.

Internally, the interlock system must transport interlock signals fast and reliably. This also includes transportation of software generated interlocks to the central interlock processor.

The interlock system must notice broken connections to interlock sources. A broken connection to an interlock source must be handled as an interlock too.

## **3.2. Processing Layer**

### **3.2.1. Description of the Central Interlock Processor**

The central interlock processing unit must condense the incoming interlock signals to summary signals which can be evaluated by the timing master [6]. These summary interlock signals will be used by the timing master to decide



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whether a beam can be handled properly or the production of the beam has to be stopped. Concentration of interlock signals has to be according to the beam production chains which are set up in the machines and to the beam mode of the beam production chains.

For each beam production chain which is set up in the machine, the interlock processing unit must summarize the interlock signals of all equipment that is used to handle this beam, and all interlock generating monitor processes which are assigned to this beam production chain. If any one equipment or monitor process signals interlock, the interlock processing unit must generate summary interlock signals.

Assignment of interlock signals to a production chain is, at first place, based on the way the beam passes through the machines, e.g. all equipment that is installed along the beam path. Additionally, further equipment and software processes that are used to produce, handle or monitor the beam have to be taken into account.<sup>2</sup>

For each beam production chain not only a single summary interlock signal has to be derived. Granularity must be at least on the level of single accelerators, but may be needed in some cases in more detail. As an example, it must be possible to stop further beam production in case of an interlock in the SIS18 but still deliver a beam which is currently accelerated in the SIS100 to the experiment.

One single incoming interlock signal often will be assigned to several beam production chains and may also be assigned to several sections of the facility. Therefore one incoming interlock signal often will be considered in several summary interlock signals.

Not always the full set of all interlock signals must contribute to the summary interlock signal:

- Depending on the beam set-up some equipment may not be needed. E.g. a beam may be set up which doesn't need a special beam manipulation RF cavity, because this type of beam manipulation is not done. In such cases, although the cavity is in the beam path, an interlock in this RF cavity must not influence the beam production chains which do not need this cavity.
- Depending on beam mode, not all interlocks from beam quality monitors should be active. E.g. for low intensity beams (pilot beams) interlock signals from the transmission monitoring system must not lead to stop further beam production und thus must not contribute to the summary interlock signal. In contrast, for normal beam production chains such interlocks must be active.

In addition, it must be possible to mask out dedicated interlock signals. However, explicitly masking interlock signals must be done with great care: It must be allowed for authorized personnel only, using standard access rights functionality provided by the main contractor. Additionally, all masking (enable/disable) of interlock signals must be logged.

To summarize, for each beam production chain which is set-up in the facility, the interlock processor concentrates the interlock inputs to summary interlock signals, as follows:

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<sup>2</sup> e.g. the orbit feedback system, the beam transmission system, the quench detection system

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- Concentrate interlock signals from all equipment, and all software processes, which take part in handling the beam (logical OR of all contributing interlock inputs). At first place all equipment along the beam path has to be taken into account, except those which are explicitly not needed (like a cooler for a non-cooled beam). In addition, superior equipment, like a feed-back system, has to be taken into account, as well as interlocks from software processes which monitor equipment or the beam quality.
- For the respective beam mode (pilot beam, production beam), don't consider those interlock signals which may be ignored for this beam mode (like bad transmission interlocks, which can be tolerated for low intensity pilot beams). Summary interlock signal generation therefore depends on the beam mode.
- Don't consider interlock sources which are explicitly masked out.
- Summary interlock signals must be specific for sections of the facility (like one accelerator or transport line).

The schema described above may be refined during the development process.

### 3.2.2. Operation of the Central Interlock Processor

It is explicitly stated that the above described schema must be handled very flexibly and will change rather frequently. Accordingly, the interlock concentration has to be carefully re-adjusted whenever the setting of the facility is modified.

Whenever the above mentioned beam setup is modified, the interlock processor must be configured specifically for each beam production chain which is set up in the facility. Configuration will be established as part of the data supply for the facility coming from the Settings Management System. The interlock system must provide an appropriate interface for dynamic configuration, which is further specified in chapter 3.2.3, especially Table 3.

The summary interlock information, as described above, must be provided to the timing master as further specified in chapter 3.2.3, especially Table 4. Based on this summary information the timing master will stop production of all affected beams in case an interlock occurs. Summary interlock information must be provided continuously to the timing master, so that the timing master can take decisions at any time.

While only specific interlock signals are used as input for the summary interlock information to be provided for the timing master, the interlock processing unit must keep track of all interlock sources in the facility.

Interlock input signals must be latched, if they are not yet latched by the interlock source. Special focus must be on interlock signals from software processes: Since such signals often are not static (as example, beam transmission will be determined once after passing of a beam pulse), the interlock system must assure that such signals are reliably recognized. Interlock input signals must be cleared by explicit reset only.

The interlock system must be represented by a software device interface (an appropriate FESA class) as any other device in the accelerator control system. At least the main functionality must be accessible by the FESA device class interface.

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The central interlock processor must archive all interlocks using a long term storage provided by the control system component Archiving System [9].

### 3.2.3. Interfaces of the Central Interlock Processor

The idea for the dynamic configuration of the interlock system is that the Settings Management System [10] manages all beam production chains and knows due to beam characteristics, which devices are needed for a given beam production chain. Based on this information, the Settings Management System generates a list of needed devices per beam production chain and provides this list to the Interlock System. Additionally, the dynamic configuration of all needed software processes for a given beam production chain must be provided. Both configurations must be changeable at runtime (and will be changed, e.g. after each scheduling change).

It is assumed that the above mentioned dynamic configuration fully suffices for the central interlock processor to concentrate incoming interlock signals and that no additional knowledge about the accelerator facility is necessary for that purpose.

At a given time, the Interlock System must hold several of such dynamic configurations: one per beam production chain and beam mode (e.g. pilot beam, production beam) combination.

The corresponding software device interface (realized by an appropriate FESA class) must support setting many dynamic interlock configurations, each characterized by the following information (“#” indicating a key of the configuration):

Part of a Configuration	Description
# Beam Production Chain	Identification of a beam production chain (i.e. to which beam production chain a given configuration belongs)
# Beam Mode	The beam mode distinguishes e.g. commissioning beam, production beam, high intensity beam, etc.
Source List	<p>A list of interlock sources that are relevant for the given beam pattern / beam production chain / beam mode combination:</p> <ul style="list-style-type: none"> <li>• relevant sections of the accelerator complex for this beam production chain</li> <li>• needed devices together with their installation location (section of the accelerator complex)</li> <li>• needed software processes together with the section of the accelerator complex for which they are relevant</li> </ul>

Table 3: Proposal for a definition of the dynamic interlock configuration (not yet complete)

The source list can contain devices, but in general could also contain identifications of software processes (since the central interlock processor also handles incoming software interlock signals, which can be masked as well). Therefore, this information is called ‘source list’ but not just ‘device list’.

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Remark: Since the interlock system supports to mask sources, these masks must be combined by the central interlock processor with the configuration described above.

The central interlock processor must provide the current interlock summary information in such a way, that the timing master can evaluate current interlocks at all times. This information contains at least:

Part of an Information	Description
# Beam Production Chain / # Beam Mode – Combination	Ok / not ok
# Beam Production Chain / # Beam Mode / # Section of the facility	Ok / not ok

Table 4: Proposal for the interlock status information for the Timing Master (not yet complete)

The Timing Master will typically check the interlock status information at each decision step within its decision trees of parallel running beam production chains. The interlock status information therefore just causes a different flow of actions within a predefined space.

Additionally to the two interfaces described above, the interlock system must present its information to the rest of the control system. This should be done via the front-end software device interface already mentioned above (same FESA class as used for the interface for the Settings Management System).

Information, which is of interest for other clients and must therefore be provided by this interface, must contain at least:

Part of an Information	Description
# Beam Production Chain / # Beam Mode – Combination	Ok / not ok
# Beam Production Chain / # Beam Mode – Combination / # Section of the facility	Ok / not ok
# Beam Production Chain / # Beam Mode – Combination	Detailed Information: Which devices are in interlock
w/o	General list of all devices / all sources, that have an interlock

Table 5: Proposal of the interlock status information for other clients (not yet complete)

### 3.3. Operation Layer

The operation layer for the interlock system mainly consists of applications that display and manage interlocks. The applications that directly belong to the interlock system are specified here. Nevertheless, other applications may also display interlock information, therefore the above mentioned interfaces must be provided.

### **3.3.1. Static Interlock Status Overview**

The Static Interlock Status Overview is part of the Interlock System. It represents a dedicated application for displaying and managing interlocks. All present Interlocks must be displayed, even those, that where masked out inside the central interlock processor. Interlocks that are masked out must be clearly visible in the application.

There must be a possibility to sort and filter interlocks by timestamp (newest / oldest first), physical machine, beam production chain and source, a dedicated functionality must support switching between relevant interlocks for operations and all interlocks (also the ones, that are masked out, just for information). Present interlocks must be clearly visible in red in such a way, that the source and the affected beam production chain or physical machine is clearly visible – even from a short distance.

It must be possible to mask out additional interlock sources within the application, they must be clearly displayed.

For all displayed interlocks, it must be distinguishable if their source is relevant for the current beam operations or not.

Since all interlocks must be acknowledged / cleared by an operator, the Static Interlock Status Overview has to provide such functionality, including a log entry into the operational logging, whenever an interlock gets cleared.

The Static Interlock Status Overview must supply two different modes:

- A Display-only mode: where interlock information is only displayed (including sorting and filtering). It must be possible to start this application many times in the FAIR accelerator complex to get an overview about present interlocks.
- A Standard mode for the use in the main control room with the full functionality (managing of interlocks, masking out interlock sources etc)

### **3.3.2. Interlock Signal Pickup Configuration Application**

The interlock system must provide interfaces to read and a GUI to visualize the signal pickup configuration of the interlock system. The Signal Pickup Configuration Application must allow to view and modify the static configuration described in chapter 3.1.

## 4. Quality Assurance, Tests and Acceptance

Generally, the software specific measures of Quality Assurance described in Common Specification "Accelerator Control System" [1] fully applies.

The system to be built must adhere to the guidelines and recommendations for software developments in the FAIR accelerator control system context, as referenced in the FAIR Common Specification F-CS-LS-01e\_ACS (Common Specification Accelerator Control System). The supplier of the work package must identify the relevant standards and recommendations before start of the development. Details must be fixed as part of the technical design concept in the initialization phase.

### 4.1. Development Methodology

The Interlock System shall be developed using an iterative approach as described in [1].

Each iteration cycle must result in a running system which can be evaluated, and tested, at FAIR site. The first iteration, which has to be available as early as possible, must concentrate on the most critical functionality. In successive iterations, the system is enhanced by adding features until the desired total functionality is reached.

In the initialization phase, the technical design concept and the plan for the iterations must be developed, and must be approved by the FAIR contracting body. At end of each iteration cycle the achieved status of the system will be evaluated and the iteration plan will be adjusted. Each iteration cycle must be approved by the FAIR contracting body before it can be started.

The realization of the Interlock System must be started with the development of a prototype including the connection of an equipment (hardware interlock source) and a front-end as well as another software process (both software interlock sources), which will be provided by the main contractor. It includes the transport of the interlock information to the central interlock processor, the concentration of interlocks taking into account a set of configurations, the notification of the timing master by a summary interlock information.

### 4.2. Quality Assurance System of the Supplier

Generally, the specific measures of Quality Assurance described in Common Specification "Accelerator Control System" [1] fully applies.

### 4.3. FAT

The FAIR Common Specification "Accelerator Control System" [1] fully applies.

### 4.4. SAT

The FAIR Common Specification "Accelerator Control System" [1] fully applies.

## **5. Documentation**

The FAIR Common Specification "Accelerator Control System" [1] fully applies.

## **6. Warranty**

The conditions and warranty period specified in the FAIR Convention applies.

## 7. Scope of Delivery

The implementation must target to support 4000 interlock sources, 2000 sources must be connected from the beginning.

No SIL (Safety Integrity Level) or PL (Performance-Level) safety levels are required for the interlock system.

The scope of delivery for the interlock system contains:

- in scope is all specific hardware of the interlock system itself, this contains:
  - local collector boxes (depending on the number of connections per local collector box, at least one local collector box will be needed per installation area, 60 installation areas are planned for FAIR)
  - all specific hardware and specific cabling for all internal connections of the interlock system
  - in scope is all specific hardware and/or cabling to connect the interlock system to the timing master
- out of scope are all cables between rooms and between buildings, they will be provided by the main supplier
- out of scope are cables towards the equipment and the terminal blocks for signal hand-over to the interlock system, both will be provided by the main supplier
- out of scope are racks. Racks will be provided by the main supplier: at maximum half a rack per installation area and one half rack centrally next to the timing master is foreseen for the interlock system
- in scope is all specific software of the interlock system, and all specific codes for programmable logic equipment, especially for
  - implementation of the interlock processor logic
  - collection of interlock signals from the equipment
  - internal communication inside the interlock system
  - interface to the timing master
  - interfaces to signal interlocks from software processes
  - interface for the dynamic configuration coming from the settings management system
  - interfaces for the applications
  - all specific drivers
- in scope are the applications specified in this document (Static Interlock Status Overview, Interlock Signal Pickup Configuration Application)
- in scope is detailed documentation of all hardware and software components

All specific software must be provided in source code. Driver software must be provided in source code, or source of supply must be provided.



## I. Attached Documents

List of abbreviations for controls (Abbreviations\_Controls.pdf).

## II. Related Documentation

- [1] F-CS-C-01e, FAIR Common Specification "Accelerator Control System"
- [2] F-TG-C-03e, FAIR Technical Guideline "Equipment Interlock and Status Signal Interface"
- [3] F-TG-C-01e, FAIR Technical Guideline "Ethernet Network Connectivity"
- [4] F-TG-C-02e, FAIR Technical Guideline "Accelerator Control System Equipment Control Interfaces"
- [5] F-TG-C-04e, FAIR Technical Guideline "Accelerator Control System Equipment Functional Requirements"
- [6] F-DS-C-05e, FAIR Detailed Specification "General Machine Timing System"
- [7] F-DG-C-03e, "Software Architecture Guideline"
- [8] F-DG-C-02e, "GUI Guideline"
- [9] F-DS-C-11e, FAIR Detailed Specification "Accelerator Control System Archiving System"
- [10] F-DS-C-03e, FAIR Detailed Specification "Settings Management System"

## III. Document Information

### III.1. Document History

Version	Date	Description	Author	Review / Approval
0.1	19. Sep 2011	Draft version	CCT	
0.2	26. Sept 2011	Draft version	Fitzek, Fröhlich	
0.2	30. Sept 2011	Draft version	Bär	
0.2	06. Oct 2011	Draft version	Krause, Fitzek, Fröhlich	
1.0	07. Oct 2011	Final draft	CCT	CCT
1.1	12. Oct 2011	Applied common structure	Fitzek	
1.2	25. Oct. 2011	Iteration of chapter 3	Krause, Fitzek, Fröhlich	
2.0	26. Oct. 2011	Final version	CCT	CCT
2.1	17. Nov. 2011	Renaming of referenced guidelines	CCT	
3.0	03. Aug. 2012	Incorporated FAIR review comments	CCT	
3.1	11. Sep. 2012	Added clarifications	Fitzek	CCT