



**Detailed Specification of the  
FAIR Accelerator Control System Component  
„Equipment Interface and Control“**

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## **Abstract**

This document is the Detailed Specification of the Equipment Interface and Control work packages “Power Supplies, Integrated Controller”, “Injection, Extraction Kicker Systems”, “RF Systems”, “Trigger Electronics” and “Custom Electronic Boards” from the hardware point of view. It covers the PSP codes 2.14.10.5.1, 2.14.10.5.2, 2.14.10.5.3, 2.14.10.5.4, 2.14.10.5.7 and 2.14.10.5.8 which are part of the “FE Systems (Device Interfaces and Controller)” work package.



## Table of Contents

1.	Purpose and Classification of the Document .....	4
1.1.	Responsibilities .....	4
1.2.	Classifications of Requirements .....	4
2.	Scope of the Technical System .....	5
2.1.	System Overview .....	5
2.2.	Limits of the System and Environment .....	6
2.2.1.	Limits .....	6
2.2.2.	Interfaces .....	6
2.3.	Environment .....	6
2.4.	Basis of Concept .....	7
2.4.1.	Functional Requirements .....	7
2.4.2.	Non-functional Requirements .....	10
2.4.3.	General Constraints .....	12
2.4.4.	Architectural Principles .....	12
3.	Technical Specifications .....	13
3.1.	Common Issues .....	13
3.2.	Front-End Controller SCU .....	13
3.2.1.	Common Features .....	13
3.2.2.	Timing Receiver Functionality .....	14
3.2.3.	Power Supply .....	14
3.2.4.	Extensibility .....	14
3.3.	Interface Electronics .....	15
3.3.1.	Digital IO Modules .....	15
3.3.2.	DAC Modules .....	15
3.3.3.	ADC Modules .....	16
3.3.4.	Timer/Counter Modules .....	16
3.3.5.	Level Adaptor Modules .....	17
3.4.	Electronic Racks .....	17
4.	Quality Assurance, Tests and Acceptance .....	18
4.1.	Development Methodology .....	18
4.2.	Quality Assurance System of the Supplier .....	18
4.3.	FAT .....	18
4.4.	SAT .....	18
5.	Documentation .....	19
6.	Warranty .....	19
7.	Scope of Delivery .....	19
8.	Acronyms and Definitions .....	20
I.	Attached Documents .....	21
II.	Related Documentation .....	21
III.	Document Information .....	21
III.1.	Document History .....	21

### List of Tables

Table 1: List of Functional Requirements for the Front-end Controller SCU .....	8
Table 2: List of Functional Requirements for the Interface Electronics .....	9
Table 3: List of Non-functional Requirements for the Front-end Controller SCU 10	
Table 4: List of Non-functional Requirements for all electronic boards including the front-end controller SCU .....	11

### List of Figures

Figure 1: System Overview of the Accelerator Control System.....	5
Figure 2: General construction of equipment interface electronics .....	6

## 1. Purpose and Classification of the Document

The purpose of this document is to specify the Accelerator Control System component "Equipment Interface and Control". This specification includes electronic components of the accelerator control system for "Power Supplies, Integrated Controller", "Injection, Extraction Kicker Systems", "RF Systems", "Trigger Electronics" and "Custom Electronic Boards" and covers the PSP codes 2.14.10.5.1, 2.14.10.5.2, 2.14.10.5.3, 2.14.10.5.4, 2.14.10.5.7 and 2.14.10.5.8.

This document is the most detailed type of document in the hierarchy of Control System specifications.

Whenever regulations and requirements are specified in the General Specifications, Technical Guidelines or Common Specifications of the Control System they are only referenced in this document. The related documents are listed in Appendix II.

No legal or contractual conditions are treated in this document. All related information is given in the General Specifications for FAIR.

### 1.1. Responsibilities

The responsibilities with respect to changes and modifications of the present document are entirely in the hands of the Controls Department of the GSI Helmholtz Centre for Heavy Ion Research GmbH (GSI) Darmstadt.

For initial information please contact the administration of the Controls Department.

Further information on the organigram, names of responsible persons and task leaders, as well as the agreed document release and approval procedure is summarized in the organizational note 'Controls Project for FAIR'.

### 1.2. Classifications of Requirements

The following definitions of requirement classifications are being used throughout the document:

- **"Must"** or **"shall"** or **"is required to"** is used to indicate mandatory requirements, strictly to be followed in order to conform to the standard and from which no deviation is permitted.
- **"Must not"** or **"shall not"** mean that the definition is an absolute prohibition of the specification.
- **"Should"** or **"is recommended"** is used to indicate that among several possibilities one is recommended as particularly suitable, without mentioning or excluding others or that a certain course of action is preferred but not required.
- **"Should not"** or **"is not recommended"** mean that there may exist valid reasons in particular circumstances when the particular behavior is acceptable or even useful, but the full implications should be understood and the case carefully weighted before implementing any behavior described with this label.
- **"May"**, which is equivalent to **"is permitted"**, is used to indicate a course of action permissible within the limits of the standard.

## 2. Scope of the Technical System

### 2.1. System Overview

The purpose of Equipment Interface and Control is to provide hardware components for controlling the FAIR accelerators. The major task of the components as specified in this document is to interface the accelerator equipment with the accelerator control system. The majority of the FAIR accelerator equipment (see Figure 1) with the exception of the beam diagnostic devices can be controlled by a dedicated front-end controller, the so-called SCU (Scalable Control Unit). The SCU is directly integrated in accelerator equipment (e.g. in power supplies) or mounted in separate electronic racks on site (see Figure 2).

The SCU is the basis for representing equipment within the accelerator control system through front-end controller software (FESA).

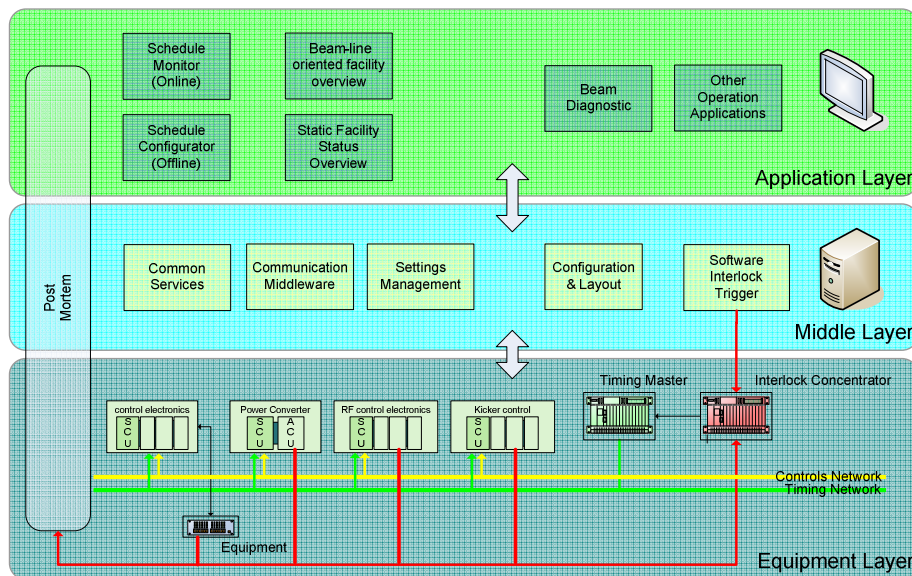


Figure 1: System Overview of the Accelerator Control System

In order to trigger and synchronize actions of equipment within the accelerator facility, the SCU provides integrated FAIR Timing Receiver Node (FTRN) functionality. FTRNs, as specified in [4], are connected to the General Machine Timing System (GMT) [3].

To interface special equipment like injection and extraction kicker systems or RF systems, dedicated electronic components are required. Those components, including trigger electronics and custom electronic boards, are summarized and specified in section 3.3. All interface electronics will be provided as SCU-Bus slave modules.

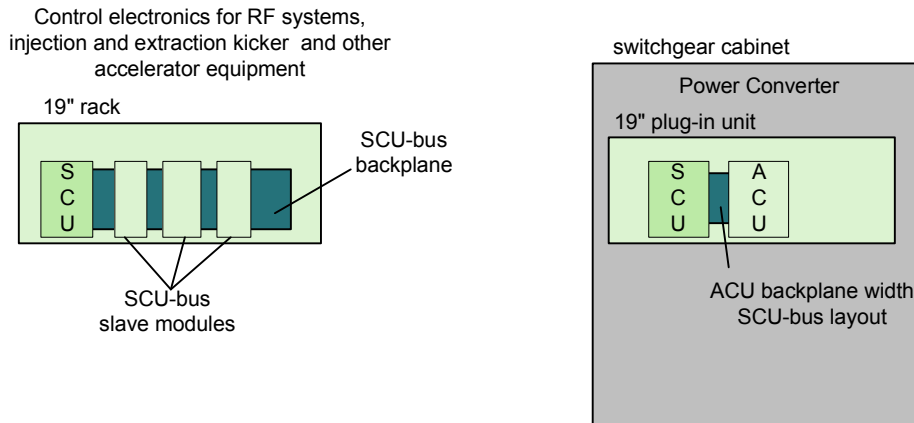


Figure 2: General construction of equipment interface electronics

## 2.2. Limits of the System and Environment

### 2.2.1. Limits

This specification does not cover the front-end software, which is realized by the FESA Front-end software framework and is specified in [7] and [8].

This specification does not cover the timing receiver nodes hosted on the SCU. Nevertheless, parts of this specification are the resources that must be provided in order to implement timing receiver functionality.

The work package Equipment Interface and Control must provide various hardware interfaces towards the equipment and towards the accelerator control system. Only the interfaces listed in [1] are supported.

### 2.2.2. Interfaces

The electronic components as defined in this specification are based on the following hardware interfaces:

- Ethernet connectivity to control system server farm with NFS [6]
- Ethernet connectivity to timing network, timing master [3]
- Parallel bus interface to the equipment [1]
- General purpose digital input-output to the equipment [1]

## 2.3. Environment

The electronic components as defined in this specification are usually mounted in the equipment (e.g. power supplies) or installed into 19" racks on site.

Unless otherwise specified, the components are designed for the following environment conditions:

- Operating temperature: +5 °C to +35 °C
- Storage temperature: 0 °C to +70 °C
- Humidity: ≤ 95 %, non-condensing.

Components are not radiation hardened and must not be installed in the tunnels, caves or locations with high radiation levels.

## 2.4. Basis of Concept

### 2.4.1. Functional Requirements

The front-end controller SCU must fulfill the following functional requirements:

Number	Description of the Requirement
EIC_010	A main CPU is required in order to host the operating system and the front-end controller software.
EIC_020	In order to implement the complete CPU functionality into the front-end controller SCU and to provide the necessary resources, a Computer-on-Module (COM) is required.
EIC_030	The SCU must provide network boot functionality in order to ease maintenance of the operating system.
EIC_040	The SCU must be able to boot the operating system and to load the front-end software without any user keystrokes.
EIC_050	For reasons of debugging, commissioning, maintenance and service a serial console is required.
EIC_060	The carrier board shall provide an FPGA with adequate speed and sufficient resources to implement hardware based functionality like equipment access, timing receiver (see [4]), and several soft core CPUs.
EIC_070	The carrier board must provide the necessary hardware resources for implementing the FTRN, especially adjustable clock sources and programmable clock rates. Further details see [4]
EIC_080	All SCUs will host an FTRN. To connect the FTRN to the timing network, a fiber optic connection is required (see [1]).
EIC_090	To connect the SCU to the accelerator controls network, a Gigabit Ethernet connection is required.
EIC_100	In order to provide additional features for diagnostic, maintenance and service a minimum of one USB interface is required.
EIC_110	A set of general purpose IOs for several application specific functionalities shall be provided. For detailed electrical specification see [1].
EIC_120	All bidirectional connectors shall be flexibly configurable as input, output, or bidirectional channel. The configuration shall be provided by a set of configuration registers inside the FPGA. The configuration should be stored in Flash or EEPROM. Prevention of short circuit of connected IOs during power-on is required.
EIC_130	Various LEDs shall be provided to allow easy commissioning, debugging and diagnostics on site. In particular, a general error LED and power good LEDs must be provided.
EIC_140	For means of communication between the SCU and the interface electronics (slave modules) the local parallel bus (SCU-Bus) must be used which is defined in [1].
EIC_150	The complete SCU-Bus interface including the arbitration must be provided as VHDL macro and should be usable on SCU-Bus slave modules.
EIC_160	The SCU interface to the SCU-Bus is the rear connector. This connector must be a VME64x 160 pin female type, see [1].

**Document Title:** Detailed Specification Equipment Interface and Control

EIC_170	The suitability for single supply operation of the whole front-end controller is required. For supply of the SCU only a single 12V-power supply is foreseen.
EIC_180	Temperature measurement on the carrier board is required. Therefore minimum of one temperature sensor shall be mounted on the board. One wire as interface is preferred.
EIC_190	For operation, maintenance, and service a clear identification of each carrier board must be provided.
EIC_200	The SCU shall be resettable via the controls network, over the rear bus interface, and by means of a reset button on the front panel which is protected against accidental use and has low sensitivity.
EIC_210	For reasons of debugging, commissioning, and service remote control shall be possible during boot-up and operation.
EIC_220	It shall be possible to update the firmware of the carrier board via the controls network, via PCIe and directly (e.g. via JTAG or USB).
EIC_230	The SCU shall provide a clock output on the rear bus interface in order to enable the clock synchronization between the Bus-Master (SCU) and the Bus-Slaves.
EIC_240	In order for the front-end software to verify correct operation, the carrier board FPGA shall have an accessible set of status registers and shall issue an interrupt if particularly critical conditions occur (e.g. lost timing synchronization, critical state in power supplies).
EIC_250	The SCU shall be able to fetch data from equipment. Therefore, a set of VHDL macros with appropriate functionality and hardware resources for triggering, synchronization and storage must be provided.

Table 1: List of Functional Requirements for the Front-end Controller SCU

The interface electronics must fulfill the following functional requirements:

Number	Description of the Requirement
EIC_310	The functionality to generate ramps of set values should generally not be implemented in the SCU. Instead, it should be hosted by the appropriate slave modules (e.g. ACU, DAC board). The slave modules must provide adequate resources in the FPGA or EPLD. For further details on the function generator see [1].
EIC_320	A set of general purpose digital or analog IOs for several application specific functionalities is required. For detailed electrical specification see [1].
EIC_340	All bidirectional connectors shall be flexibly configurable as input, output, or bidirectional channel. This configuration shall be provided by a set of configuration registers inside the FPGA. The configuration should be stored in Flash or EEPROM. Prevention of short circuit of connected IOs during power-on is required.



**Document Title:** Detailed Specification Equipment Interface and Control

EIC_350	A Din41612-connector as rear interface (female, 96 pin) is required. The connector realizes the backplane connectivity. This is the predefined standard parallel bus interface to communicate with the equipment via SCU-Bus slave modules, see [1].
EIC_360	In case of using the extended parallel bus interface, a VME64x 160 pin female type rear connector is required. The extended version offers a set of optional IO functions.
EIC_370	In order for the front-end software to verify correct operation, each slave module shall have an accessible set of status registers and shall issue an interrupt if particularly critical conditions occur (e.g. FPGA lost configuration, critical state in power supplies, RF device lost synchronization).
EIC_380	Various LEDs shall be provided to allow easy commissioning, debugging and diagnostics on site. In particular, a general error LED and power good LEDs must be provided.

Table 2: List of Functional Requirements for the Interface Electronics

### 2.4.2. Non-functional Requirements

The front-end controller SCU must fulfill the following non-functional requirements:

Number	Description of the Requirement
EIC_410	<b>Extensibility -</b> For several application-specific expansion cards a suitable connector type shall be available. The signal design shall ensure that as many carrier board resources as possible are accessible.
EIC_420	<b>Scalability -</b> Mainly due to the COM Express™ module, scalability of the SCU is achievable. The mechanical design shall allow using different COM Express™ modules. As system memory SO-DIMM RAM modules are preferred.
EIC_430	<b>Thermal Design Power -</b> Under thermal aspects the thermal design power of the whole SCU must be less than 35 W.

Table 3: List of Non-functional Requirements for the Front-end Controller SCU

All electronic boards including the SCU must fulfill the following non-functional requirements:

Number	Description of the Requirement
EIC_510	<b>Testability -</b> Testability aspects must be considered during the whole design phase. The contractor shall provide the required test software and an appropriate test environment. Test conditions must be defined well.
EIC_520	<b>Real time reliability –</b> The design of all interface electronics must take into account the local delays of actions connected to relevant events, in order to guarantee timely execution or to signal a missed deadline.
EIC_530	<b>Identification of hardware and firmware –</b> The front-end controller and every interface electronic board shall provide a unique serial number, model and revision. Each firmware shall provide type and version number. This information shall be accessible by a set of registers.
EIC_540	<b>ESD protection –</b> For reasons of ESD protection the circuit design shall take reasonable precautions for all user IOs (digital and analog). This applies especially to the free accessible front interfaces.
EIC_550	<b>Cooling Concept –</b> The mechanical design must ensure that passive heat dissipation is sufficient. Fans inside the modules to realize forced air cooling must not be used.

**Document Title:** Detailed Specification Equipment Interface and Control

EIC_560	<p><b>Grounding –</b> Metallic parts like the front plate must connect to the chassis ground (protective earth). Therefore the layout shall provide a separate ground area. An optionally low resistance connection between signal ground and chassis ground should be feasible as easy as possible.</p>
EIC_570	<p><b>Signal grounds –</b> The SCU-Bus backplane has separate layers of digital and analog ground. Also the pinning of the modules' rear connector has separated ground pins. In case of modules with analog functionality the digital ground and the analog ground must be connected. These potentials must be connected only on one point. The connecting point should be located as near as possible to the rear connector. For reasons of EMC ground loops must be avoided and low inductive ground connections must be realized.</p>
EIC_580	<p><b>Utilization of electronic components –</b> Concerning the durability of the electronic modules, the design shall respect the electrical and thermal utilization of electronic components. It is strongly recommended to utilize electronic components with a maximum of 80% of their rated values. Electrolytic capacitors shall be used with a maximum of 50% of their rated voltage.</p>
EIC_590	<p><b>Thermal utilization –</b> Concerning durability of electronic components it is strongly recommended to use components with rated operating temperature of at least 85 °C only.</p>

Table 4: List of Non-functional Requirements for all electronic boards including the front-end controller SCU

### **2.4.3. General Constraints**

#### **Computer-on-Module**

Because of the availability and distribution in industrial applications COM Express™ is preferred. Concerning the mechanical design the form factor "compact" is required. For software compatibility reasons an x86 based system is mandatory.

#### **Network boot functionality**

PXE boot functionality is necessary. Dedicated front-end controllers in the accelerator control system will load the operating system by PXE boot request.

#### **Embedded BIOS and Boot Up behavior**

An Embedded BIOS with the ability for headless operation is required. This ensures boot-up functionality without any user key strokes. For reasons of debugging, commissioning, maintenance and service a remote console is required and must be implemented by using a BIOS virtual terminal.

#### **Gigabit Ethernet**

Usually a twisted pair copper cable is connecting the SCU to the accelerator controls network. Therefore one RJ45 connector is mandatory.

#### **Technical Guidelines**

The Technical Guideline [1] and [2] fully applies.

### **2.4.4. Architectural Principles**

All of the specified electronic components are designed for installation in 19"-racks. The following design principles for the components must be applied.

Scalable Control Unit (SCU):

- Stacked design (sandwich); carrier board and COM
- 19"-cassette as housing, 14 HP width, 3 U height
- Front interface for copper and fiber channel Gigabit Ethernet, USB, RS-232, general purpose digital IO, Reset-Button, diagnostic LEDs

Trigger electronics and custom electronic boards (summarized as interface electronics):

- 100x160 mm<sup>2</sup> Eurocard width rear connector, DIN 41612, 96 pins or VME64x, 160 pins if required
- Front interface for user IO (general purpose digital IO, or analog IO, or both), diagnostic LEDs, Reset-Button (if required and useful)
- Front cover, 4 HP width, 3 U height

## **3. Technical Specifications**

### **3.1. Common Issues**

Each electronic board shall provide a unique serial number coded in hardware.

A Mean Time Between Failure (MTBF) calculation for each interface electronic board shall be performed by the contractor.

The mechanical design shall allow quick replacement of boards or modules on site.

All boards or modules should have LEDs at least to display debug or error information.

All boards or modules with configurable electronic components (like FPGA, EPLD, etc.) shall have a reset button.

All schematics and components on different boards or modules with comparable functionality should be as similar as possible.

All integrated circuits and other electronic components shall be available from second source.

### **3.2. Front-End Controller SCU**

The main components of the SCU are a carrier board with an adequate powerful FPGA and an of-the-shelf Computer-On-Module (COM). A standardized COM Express™ module as COM is to be favored. A processor system in x86 architecture is mandatory.

The physical interface for the BIOS virtual terminal should be a conventional RS 232 interface.

Real time actions, data acquisition and other time critical tasks will be provided by the carrier board electronics. Especially the FTRN functionality is mainly realized by the FPGA.

#### **3.2.1. Common Features**

The mechanical architecture of the carrier board must meet the requirements of a Eurocard with rear plug-in connector (in dependence on IEEE 1101.10). The rear connector realizes the backplane connectivity via VME64x connector with 160 pins. The interface and pinning is defined in [1].

The rear interface is a parallel bus, the so-called SCU-Bus. The SCU-Bus is the standard interface to communicate through the slave modules with the equipment.

Furthermore, several general purpose digital IOs are provided.

For the communication between the carrier board and the COM, PCI-Express is to be favored. Interrupt support is mandatory. All carrier board resources should be represented as PCI device.

For operation, maintenance, and service a clear identification of each carrier board is necessary.

### **3.2.2. Timing Receiver Functionality**

The SCU acts as an FTRN in the FAIR Timing network. Therefore the carrier board shall provide the necessary hardware resources. The White Rabbit core will be implemented in FPGA (see [4] for further details).

The FTRN must have the following features:

- a clock synchronized with a clock master with at least 1 ns accuracy
- ability to generate event write cycle on the parallel bus interface (SCU-Bus) at given times
- ability to generate a digital pulse or a pulse sequence at a given time
- ability to generate clock signals with a given frequency and phase
- ability to generate specified interrupts at given times

### **3.2.3. Power Supply**

As power supply unit for the front-end controller a single 12-V-supply is available. So the carrier board has to generate all the required voltage levels of power supply on board by itself.

The thermal design power of the carrier board must be less than 20 W.

### **3.2.4. Extensibility**

The carrier board shall provide an expansion slot. Using an extension board the SCU will optionally be able to provide additional functionality, such as the GSI device-bus (MIL-STD-1553B like), additional serial high-speed channels and auxiliary digital or analog IOs.

### **3.3. Interface Electronics**

A set of electronic boards will be provided as SCU-Bus slave modules. The common interface for the Bus-Master (SCU) and the slave boards is the SCU-Bus as specified in [1].

The SCU-Bus realizes a master-slave architecture. The SCU is the bus master and supports up to 12 slave modules.

The technical parameters and characteristics of each module shall be specified in a detailed technical module specification and approved by the contracting body.

#### **3.3.1. Digital IO Modules**

Digital IO modules shall provide up to 32 general purpose digital IO lines, usually distributed on the rear interface. In case of a front interface, digital IO modules shall provide up to 8 IO channels. The logic state and direction of each channel shall be indicated by LEDs.

The interface variants depend on the application and can be TTL, LVTTTL, 50 Ohm-line interface, or PLC 24 V DC I/O [1].

All bidirectional IO lines shall be flexibly configurable as input, output, or bidirectional channel.

For digital outputs short-circuit withstand capability is usually required.

The circuit design should allow the configuration of direction for pin groups of at least 4 channels. Configuration of direction of each single channel is not necessary.

The configuration shall be provided by a set of configuration registers inside the FPGA. The configuration should be stored in Flash or EEPROM.

Prevention of short-circuit of connected IOs during power-on is required.

For reasons of ESD protection the circuit design shall take reasonable precautions for all user IOs (digital and analog). This applies especially to the free accessible front interfaces.

For the whole signal transmission a few nanoseconds should not be exceeded. The delay and latency time must be calculable and repeatable.

#### **3.3.2. DAC Modules**

Digital/analog converter modules will be used mostly to generate analog setpoints for the equipment.

Such DAC-modules are providing one or two channels with a resolution of 16 bit. The nonlinearity and accuracy depends on the module design and the requirements of the application.

The output channels provide by default a voltage interface with  $\pm 10$  V. Other interface variants like current loop (0-20 mA, 4-20 mA) or voltage levels (e.g.  $\pm 5$  V) should be available [1].

The power supply (  $\pm 15$  V, +5 V) will be provided by the SCU-Bus-backplane.

**Document Title:** Detailed Specification Equipment Interface and Control

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Usually the analog channels are provided on the front panel of the module.

An FPGA to control and configure the module is mandatory. The FPGA provides the function generator for each analog channel. Sufficient resources concerning memory space and timing requirements must be provided.

**3.3.3. ADC Modules**

ADC-modules will be used to measure miscellaneous process values. These modules do not support beam diagnostic functionality.

Such modules should provide up to 8 channels of analog input. The default input voltage range is  $\pm 5$  V or  $\pm 10$  V. The input impedance is greater than 1 M $\Omega$ . Usually, differential channels will be available which are provided on the front panel of the module.

The resolution shall be 12 bit up to 16 bit and the conversion time shall be shorter than 4  $\mu$ s [1].

The possibility of external triggering is mandatory. Separate triggering for each channel is not necessary. Continuous sampling should be configurable.

The power supply (  $\pm 15$  V, +5 V) will be provided by the SCU-Bus-backplane.

An FPGA to control and configure the module is mandatory. The FPGA supports data acquisition functionality. Sufficient resources concerning memory space and timing requirements must be provided. A minimum of 1 MB memory per channel is required.

**3.3.4. Timer/Counter Modules**

A special variant of digital IO modules is realized as timer/counter module. These modules should provide functionality as follows:

- trigger inputs
- pulse outputs
- general purpose digital inputs and outputs
- multi pulse generation
- delay generation
- counter functionality with capture and compare functionality

An FPGA to control and configure the module is mandatory. The FPGA provides the above functionality. Sufficient resources concerning memory space and timing requirements must be provided.

For digital outputs short-circuit capability is usually required. For the whole signal transmission a few nanoseconds should not be exceeded. The delay and latency time must be calculable and repeatable.



### **3.3.5. Level Adaptor Modules**

Interfaces for controlling the equipment and gathering process information might be incompatible. In this case, it is necessary to provide a set of level adaptor modules. The levels and values depend on the equipment.

## **3.4. Electronic Racks**

The control hardware for the accelerator equipment like magnet power converters, ring RF, kickers etc. are mounted in 19" racks.

Each rack is equipped with a backplane, power supplies, main switch, usually one SCU (as bus master), and slave boards (electronic modules as described above or other equipment-specific slave boards).

Generally, the racks contain the following components:

- 19" rack, unit height 3 U, IEEE 1101.1 compatible
- parallel bus backplane
- power supply units for the whole crate, 5 V, 12 V and 15 V if needed
- SCU module
- electronic modules as described above or other equipment-specific slave boards

The backplane shall be available in two variants. A long sized backplane for up to 12 bus-slaves and a short variant with up to five slave-slots.

So in principle there is the possibility to equip one 19" rack with two SCU modules and up to five slave-boards per SCU.

In case of magnet power supplies, the backplane differs from the standard SCU-Bus backplane in the mechanical point of view.

The so-called ACU-backplane provides the same signal-layout as the default SCU-Bus backplane.

For further details and requirements, see [1].

## **4. Quality Assurance, Tests and Acceptance**

The system to be built must adhere to the guidelines and recommendations for software developments in the FAIR accelerator control system context, as referenced in the FAIR Common Specification (Common Specification Accelerator Control System, [5]). The supplier of the work package must identify the relevant standards and recommendations before start of the development. Details must be fixed as part of the technical design concept in the initialization phase.

### **4.1. Development Methodology**

The FE systems as defined in this document shall be developed in a commonly accepted methodology for industrial electronic development.

The main steps are as follows:

- Conceptual design
- Development of the schematic diagram
- Fine design and worst case calculation
- Prototyping, type check and redesign if necessary
- Engineering samples manufacturing
- Field test and long-term test
- Pre-series manufacturing
- Series production
- Installation and commissioning on site

An adequate documentation of each step is necessary.

### **4.2. Quality Assurance System of the Supplier**

Generally, the hardware specific measures of Quality Assurance described in Common Specification "Accelerator Control System" [5] fully applies.

### **4.3. FAT**

The Common Specification "Accelerator Control System" [5] fully applies.

### **4.4. SAT**

The Common Specification "Accelerator Control System" [5] fully applies.

## **5. Documentation**

The Common Specification "Accelerator Control System" [5] fully applies.

## **6. Warranty**

The conditions and warranty period specified in the Contract applies.

## **7. Scope of Delivery**

The contractor shall deliver the following goods:

- Detailed technical specifications of the SCU and each electronic module, including technical data of hardware, specification of firmware, and drivers.
- Fully disclosed development work for all modules.
- Drivers for host system CPUs. The primary operating system is Linux.
- HDL and tools sufficient to synthesize firmware regarding the modules.
- Module specific test facilities, allowing automated tests of a large number of modules in the shortest possible time.
- Test programs with the capability for debugging, commissioning, maintenance and service of each module.
- Approximately 1500 SCUs, approximately 150 electronic racks (see 3.4) and the required number (roughly 200) of interface electronic boards (see 3.3)
- Documentation for all deliverables.

## 8. Acronyms and Definitions

The following acronyms and definitions are used in this document.

- **ACU** - Adaptive Control Unit
- **ADC** - Analog-to-Digital Converter
- **BEL** - GSI Accelerator Controls and Electronics Department
- **COM** - Computer-On-Module
- **DAC** - Digital-to-Analog Converter
- **EEPROM** - Electrically Erasable Programmable Read-Only Memory
- **EMC** - Electromagnetic Compatibility
- **EPLD** - Erasable Programmable Logic Device
- **ESD** - Electrostatic Discharge
- **FAT** - Factory Acceptance Test
- **FEC** - Front-end Controller
- **FESA** - Front-end Software Architecture
- **FPGA** - Field Programmable Gate Array
- **FTRN** - FAIR Timing Receiver Node
- **IO** - Input-Output
- **JTAG** - Joint Test Action Group, standardized as the IEEE 1149.1
- **LVTTTL** - Low-Voltage-TTL
- **MTBF** - Mean Time Between Failure
- **NFS** - Network File System
- **PCI** - Peripheral Component Interconnect
- **PLC** - Programmable Logic Controller
- **PXE** - Preboot eXecution Environment
- **SAT** - Site Acceptance Test
- **SCU** - Scalable Control Unit
- **TTL** - Transistor-transistor logic

## I. Attached Documents

List of abbreviations for controls (Abbreviations\_Controls.pdf).

## II. Related Documentation

- [1] F-TG-C-02e, FAIR Technical Guideline "Control System Equipment Interfaces"
- [2] F-TG-ET-01e, FAIR Technical Guideline "Electrical Design Rules and Regulations"
- [3] F-DS-C-05e, FAIR Detailed Specification "General machine timing system"
- [4] F-DS-C-06e, FAIR Detailed Specification "Timing Receivers"
- [5] F-CS-C-01e, FAIR Common Specification "Accelerator Control System"
- [6] F-DS-C-26e, FAIR Detailed Specification "Controls IT environment, part 2 (network)"
- [7] F-DS-C-01e, FAIR Detailed Specification "FEC Software Framework (FESA)"
- [8] F-DS-C-28e, FAIR Detailed Specification "Equipment control software"

## III. Document Information

### III.1. Document History

Version	Date	Description	Author	Review / Approval
0.1	16.3.2012	Draft	M. Thieme	
0.2	20.3.2012	Draft	CCT, M. Thieme	
0.3	23.3.2012	Draft	CCT, M. Thieme	
0.4	19.04.2012	Draft	CCT, M. Thieme	
1.0	20.04.2012	Final version	M. Thieme	CCT
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